**Layout instructions for 31-0002 (Ghost River)**

Schematic: 33-0002

Assembly: 30-0002

Artwork/Raw PCB: 31-0002

CAD files (PADs): 34-0002

Pallet drawing (if applicable): 32-0002

General board requirements:

PCB material and thickness: 0.062” thick; FR-4; 1-ounce CU clad; ENIG

Rough shape: 40mm X 16.5mm

Layers: 4

Layer designations:

1: Top components and routes

2: Plane (GND\_SIGNAL)

3: Plane (VCC)

4: Bottom components and routes

Component placement:

See drawing (PCB, SoS MECHANICAL). The locations of the connector (J1), the photodiode (D1) and the 4 mounting holes are fixed. The rotational orientation of D1 are at the designer’s discretion.

Component placement and critical routes:

* The power filtering section components (C1, C2, C3, C4 and L1) should be placed on both sides in the area between the top of the board (as shown in the mechanical drawing) and the first pair of mounting holes. The traces between these devices should be kept to a minimum length and as wide as reasonable (25mils). The routes for C2 and C4 are the most important as these will deal with any high frequency noise. The route from J1-P1 is not as critical for length or width.
* Where possible multiple vias (2-4) should be used when connecting to the plane layers for filtering and decoupling caps
* U1, C5 and R3 should be placed in close proximity to the photodiode (D1). The routes between these components should be kept a short as reasonable and not use vias. The trace widths should be between 15 and 20 mils to keep the inductance to a minimum while keeping parasitic capacitance to a minimum as well. The plane layer below these components should be (GND\_SIGNAL).
* As per usual, the decoupling caps (C8 and C11) should be placed as close to their ICs as possible with thick traces to keep the inductance to a minimum.
* The mounting holes should be connected together in a “ring” using a hefty trace(25 to 50 mils) to minimize inductance. The should be done on both the top and the bottom with vias spaced in 0.10 mil increments
* Resistors R1 and R2 should be placed near J1 with minimal trace length to the ground ring. R2 should have multiple vias (2-4) to the ground plane